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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. END920000132US1

In Re Application Of: **Mark L. Janecek et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/853,506	05/11/2001	Jose H. Alcala	2827

Invention: **CIRCUIT BOARD CONSTRUCTION**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Signature

Dated: **5/29/03**

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Mark Levy

Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:	) Art Unit: 2827
Mark L. Janecek et al.	) Examiner: Jose H. Alcala
Serial No.: 09/853,506	) Date: May 23, 2003
Filed: May 11, 2001	) Attorney Docket No.:) END920000132US1
For: CIRCUIT BOARD CONSTRUCTION	))

APPEAL BRIEF

Honorable Commissioner of Patents and Trademarks

Washington, DC 20231

S I R:

This Appeal is taken from the FINAL REJECTION of claims 1, 2, 4 through 7, 11, 12, and 14, as presented in the Office Action of December 4, 2002 (Paper No. 8), for the above-identified application.

The Commissioner is hereby authorized to charge any fees in connection with this appeal or with other matters before the USPTO, to the undersigned's Deposit Account No. 19-0077.

REAL PARTY IN INTEREST

The real party in interest hereto is Appellants' assignee. The interest in the invention was assigned by the inventors to International Business Machines Corporation at the time of filing the application, and was recorded on Reel No. 011817, Frame No. 0241.

RELATED APPEALS AND INTERFERENCES

This appeal is the first appeal before the Office.

STATUS OF THE CLAIMS

All of the presently pending claims 1, 2, 4 through 7, 11, 12, and 14, now stand FINALLY REJECTED as of December 4, 2002 (Paper No. 8), which was reaffirmed in the Advisory Action of April 23, 2003.

The rejection of claims 1, 2, 4 through 7, 11, 12, and 14 is hereby appealed.

STATUS OF THE AMENDMENTS

The subject patent application was filed on May 11, 2001. An Office Action rejecting claims 1 through 10 was mailed on September 10, 2001 (Paper No. 2). An Amendment was filed on January 10, 2002. An Office Action rejecting claims 1 through 7 and 11 through 14 was mailed on May 8, 2002 (Paper No. 5). An Amendment was filed on September 16, 2002. A Final Office Action rejecting claims 1, 2, 4 through 7, 11, 12, and 14 was mailed on December 4, 2002 (Paper No. 8). An Amendment was filed on March 11, 2003. An Advisory Action affirming the rejection of claims 1, 2, 4 through 7, 11, 12, and 14 was mailed on April 23, 2003. Applicants filed a Notice of Appeal on May 2, 2003.

SUMMARY OF THE INVENTION

The invention features a circuit board laminate comprising an inner power core that is connected between two signal cores. Upon lamination of the cores, the circuit board structure is electrically connected. The laminated circuit board inner power core comprises filled via through holes of conductive adhesive. The conductive power core vias make contact with the metal pads of the conductive vias of the respective outer signal cores, upon lamination.

ISSUES

Should claims 1, 2, 4 through 7, 11, 12, and 14 have been rejected under 35 U.S.C. §102(b) as anticipated by DiStefano et al?

GROUPING OF THE CLAIMS

It would appear that all the claims can be grouped together.

ARGUMENTS

If it pleases the Honorable Board, the rejection of the claims over DiStefano et al, is not tenable. At first blush, it would appear that the reference to DiStefano et al is anticipatory to the claimed structure recited in the claims. Upon careful analysis, however, one is able to perceive a major inconsistency between the claimed invention and the cited reference.

Referring to the most basic structure of DiStefano et al, as shown in FIGURE 2, the first, or top layer 16 is shown with a plated through hole via 22 as is the third layer 16

with plated through hole via 22, which appears to be aligned with the first via 22.

The difference between the claimed invention and that of the cited patent to DiStefano et al lies with the second, or intermediate layer. The second layer, which is described in DiStefano et al, as an interposer 12, comprises flowable dielectric layers 38 and 40 that encase the interior element 42 that can be fiber or glass (column 15, lines 39 through 43 and column 16, lines 10 through 23). The interposer or second layer 12 is not designed as a power core layer. Neither does this layer have a distinct plated via through hole that aligns with plated via through holes of the first and second layers. If a reference fails to describe all components of a claim, it fails as a reference. Minnesota Mining and Manufacturing Co. v. Johnson & Johnson Orthopedics Inc., 24 USPQ2d 1321, 1326(Fed. Cir. 1992); Apple Computer, Inc. v. Articulate Systems, Inc., 57 USPQ2d 1057, 1061 (Fed. Cir. 2000). One merely has to read further and observe the amorphous, flowable structure of the interposer layer shown in FIGURE 3, 4, 5, etc., to realize the non-alignment of the hole (via) of the second, or interposer layer with the plated vias of either the first or third layers. The hole structures, however they may be described (plated vias or just plain holes), are not distinctly described as aligned by DiStefano et al, but merely as matched. This is corroborated by the subsequent FIGURES 3, 4, 5, etc. Drawings are

integral parts of patents and can be used to show how elements are connected. Autogiro Co. of America v. United States, 384 F.2d 391, 398, 155 USPQ 697, 703 (Ct. Cl. 1967).

In addition, because dielectric elements 38 and 40 are flowable, it is not possible that the interposer layer can properly be described as making the alignment of the vias by way of lamination.

The distinction is quite clear with reference to FIGURES 1 through 3, of Appellants' FIGURES, and to Appellants' independent claims 1, 5, and 11. These claims recite the alignment of the vias in all three layers. In addition, claim 5 describes holes, whose conductive pads are slightly undercut. There is simply no such recitation in the text of DiStefano et al.

In summary, the patent to DiStefano et al fails to show, teach, or textually describe: (1) a power core (intermediate) layer, (2) a second or intermediate layer with distinctly plated via holes that are distinctly aligned with the other two signal core layers, or (3) the undercut pads of the power core layer that aligns with the vias of the adjacent signal core layers. Only one element missing from a reference is sufficient to show patentability; two or more missing elements are clearly probative. Brown v. 3M Systems Inc., 60 USPQ2d 1375, 1376 (Fed. Cir. 2001).

CONCLUSION

The Honorable Board is respectfully requested to reverse the rejection to claims 1, 2, 4 through 7, 11, 12, and 14, and allow the application to issue.

Respectfully submitted,

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Commissioner of Patents and Trademarks
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on 5/29/03 (Date of Deposit)

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APPENDIX

1. (Amended) A three-layered, laminated circuit structure, comprising:

a first substrate having conductive via through holes disposed therein;

a second substrate laminated to said first substrate and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first substrate; and

a third substrate laminated to said second substrate having via through holes that align with, and make electrical contact with, the adhesive filled via through holes of said second substrate, thus forming said three-layered, laminated circuit structure.

2. (Twice Amended) The three-layered circuit structure in accordance with claim 1, wherein said first and third substrates each comprise a signal core layer, and said second substrate comprises a power core layer.

3. (Amended & Cancelled) The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a pair of spaced-apart outer signal cores, and said second substrate comprises an inner power core sandwiched between said pair of spaced-apart outer signal cores.

4. (Twice Amended) The three-layered circuit structure in accordance with claim 2, wherein said via through holes of said power core layer comprises undercut contact surfaces, and said via through holes of each of said signal core layers have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said power core layer.

5. (Amended) A multi-layered circuit structure, comprising:

a first substrate having conductive via through holes disposed therein; and

a second substrate laminated to said first substrate, and having via through holes comprising conductive adhesive coated pads that align with, and make electrical contact with, the conductive via through holes of said first substrate.

6. (Twice Amended) The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a signal core layer, and said second substrate comprises a power core layer.

7. (Twice Amended) The multi-layered circuit structure in accordance with claim 5, further comprising a third substrate having similar structure to that of said first substrate, said first and third substrates each being laminated to said second substrate, and wherein said first and third substrates each define a signal core layer, said second substrate further defining an inner power core layer sandwiched between each of said signal core layers.

8. (Cancelled) A method of fabricating a multi-layered circuit, comprising the steps of:

filling via through holes of a first substrate with conductive adhesive;

aligning said via through holes of said first substrate with conductive via through holes of a second substrate; and

laminating together said first and second substrates.

9. The method in accordance with claim 8, wherein said first substrate comprises a signal core layer, and said second substrate comprises a power core layer.

10. (Cancelled) The method in accordance with claim 8, wherein said first substrate comprises a pair of outer signal core layers, and said second substrate comprises an inner power core layer sandwiched between said pair of outer signal core layers.

11. (Added & Amended) A multi-layered circuit structure, comprising:

first and second substrates, each having conductive via through holes disposed therein; and

a third substrate laminated between said first and second substrates and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first and second substrates.

12. (Added & Amended) The multi-layered circuit structure in accordance with claim 11, wherein said first and second substrates each comprise a signal core layer, and said third substrate comprises a power core layer.

13. (Added & Cancelled) The multi-layered circuit structure in accordance with claim 11, wherein said first substrate comprises a pair of spaced-apart outer signal cores, and said second substrate comprises an inner power core sandwiched between said pair of outer signal cores.

14. (Added & Amended) The multi-layered circuit structure in accordance with claim 12, wherein said via through holes of said inner power core layer comprise undercut contact surfaces, and said via through holes of each of said signal core layers each have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said power core layer.